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Atty. Dkt. No. 040405-0368

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Atsufumi SHIBAYAMA et al.
Title: PROGRAM PARALLELIZATION DEVICE, PROGRAM
PARALLELIZATION METHOD, AND PROGRAM
PARALLELIZATION PROGRAM
Appl. No.: 10/811,925
Filing Date: 03/30/2004
Examiner: Chaki, Kakali
Art Unit: 2193
Confirmation Number: 3161

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56

Mail Stop PATENT APPLICATION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56.

A copy of each non-U.S. patent document and each non-patent document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.



TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(b), before the mailing date of the first Office Action on the merits, and within three (3) months of the mailing date of the foreign office communication.

RELEVANCE OF EACH DOCUMENT

The documents listed on the attached PT0/SB/08 were cited as being relevant during the prosecution of the corresponding Japanese application. A partial English translation of the Japanese Office Action of August 22, 2006, follows:

Note (for the cited literature, see the List of Cited Literature)

- Claims 1–5, 8, 9, 12, 13, 16, and 17–20
- Cited literature 1
- Remarks

Cited Literature 1 describes an invention wherein all branching instructions are examined as fork candidates, those for which the fork boost value exceeds a set value are converted into fork instructions, a performance evaluation is carried out, and suitable fork locations are evaluated. There is no remarkable difference between the inventions according to Claims 1–5, 8, 9, 12, 13, 16, and 17–20 of the present application and the invention described in Cited Literature 1.

(3) The inventions related to the following claims of the present application could have been easily invented by a person with ordinary knowledge of technology in the field to which the inventions belong prior to the filing of this application based on the inventions recited in the publications below, which had been distributed in Japan or abroad, or inventions which became publicly available via telecommunication lines, prior to the filing of this application, and therefore cannot receive a patent according to the stipulations of Article 29, Paragraph 2 of the Japan Patent Law.

Note (for the cited literature, see the List of Cited Literature)

- Claims 1–5, 8, 9, 12, 13, 16, and 17–20
- Cited literature 1
- Remarks

Cited literature 1 describes an invention as examined already under reason (2), and making the inventions relating to Claims 1–5, 8, 9, 12, 13, 16, and 17–20 of the present application based on this description is a matter which could be easily conceived of by a person skilled in the art.

If any reasons for rejection are newly discovered, a Notification of Reasons for Rejection will be issued.

List of Cited Literature

1. Junji Sakai and 6 others: Automatic parallel compiling techniques for control parallel architecture. 1998 Parallel Processing Symposium, Japan, Information Processing Society, June 3, 1998, Vol. 98, No. 7, pages 383 through 390 (CSDB number: CS-NG-2001-00091-041). See especially the sections “4.2 Selecting fork locations” on pages 386 through 387, “Effects of fork threshold” and “Branching types” on page 389, and “Tuning of fork destination” on pages 389 through 390.

Record of Prior Art Literature Search Results

- Fields searched IPC G06F 9/45

G06F 9/46 – 9/54

- Prior art literature Japanese Unexamined Patent Application Publication H10-027108

Japanese Unexamined Patent Application Publication H10-078880

Japanese Unexamined Patent Application Publication 2003-029984

Japanese Unexamined Patent Application Publication 2003-029985

Japanese Unexamined Patent Application Publication 2001-282549

Jun Torii and 5 others: Proposal for the on-chip control parallel processor MUSCAT. Joho Shori Gakkai Ronbunshi, Japan, Information Processing Society, June 15, 1998, Vol. 39, No. 6, pages 1622 through 1631 (CSDB No.: JP-N4-03-09736)

This Record of Prior Art Literature Search Results does not constitute a reason for rejection.

Document C1 is a U.S. counterpart of Document C2. Copies of Documents C3-C6 are not provided herewith, as copies of these documents were submitted with Applicant's Information Disclosure Statement of March 30, 2004.

Any document listed on the attached PTO/SB/08 was cited as being relevant during the prosecution of the corresponding Japanese application

Applicant's statements regarding the Japanese Office Action are based on a partial translation that Applicant's representative obtained. These statements should in no way be considered as an agreement by Application with, or an admission of, what is asserted in the Japanese Office Action.

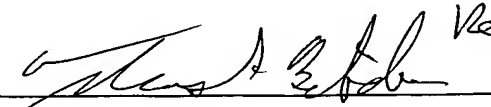

Applicants respectfully request that each listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

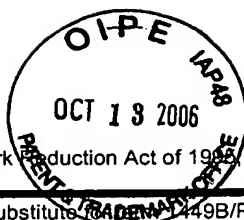
Although Applicant believes that no fee is required for this Request, the Commissioner is hereby authorized to charge any additional fees which may be required for this Request to Deposit Account No. 19-0741.

Respectfully submitted,

Date: October 13, 2006

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MODIFIED PTO/SB/08 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute Form 149B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: October 13, 2006 (use as many sheets as necessary)		Complete if Known	
		Application Number	10/811,925
Sheet 1 of 1		Filing Date	03/30/2004
		First Named Inventor	Atsufumi SHIBAYAMA
		Group Art Unit	2193
		Examiner Name	Chaki, Kakali
		Attorney Docket Number	040405-0368

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
	C1	2003/0014471	A1	OHSAWA et al.	01-16-2003	

UNPUBLISHED U.S. PATENT APPLICATION DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Application Document		Name of Patentee or Applicant of Cited Document	Filing Date of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Serial Number	Kind Code ² (if known)			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
	C2	JP	2003-029984	A	NEC CORPORATION	01-31-2003		A
	C3	JP	2003-029985		NEC CORPORATION	01-31-2003		A
	C4	JP	2001-282549		NEC CORPORATION	10-12-2001		A
	C5	JP	10-078880		NEC CORPORATION	03-24-1998		A
	C6	JP	10-027108		NEC CORPORATION	01-27-1998		A

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	C7	J. SAKAI et al., "Automatic parallel compiling techniques for control parallel architecture," 1998 Parallel Processing Symposium Japan, Information Processing Society, June 3, 1998, Vol. 98:7, pp. 383-390.	
	C8	J. TORII et al., "Proposal for the on-chip control parallel processor MUSCAT," Information Processing Society, June 15, 1998, Vol. 39:6, pp. 1622-1631.	

Examiner Signature

Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.